15W, 12V RF Power LDMOS FETs

Description

The ITSN20015P2 is a common source N-channel, enhancement-mode lateral field-effect RF power transistor. It is designed for high gain, broadband commercial and industrial applications, with frequencies up to 2 GHz.

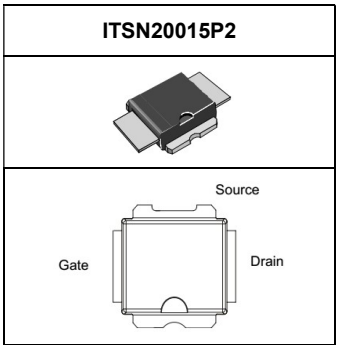


Figure 1. Pin Connection

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 12 Volts, I_{DQ} = 300 mA，CW.

Frequency (MHz)	Gp (dB)	P_1dB (W)	η_D (%)	P_3dB (W)	η_D (%)
870	16.4	18	56	22	60

- Typical Performance (On Innogration fixture with device soldered):

V_{DD} = 12 Volts, I_{DQ} = 350 mA，CW.

Frequency (MHz)	Gp (dB)	P_1dB (W)	η_D (%)	P_3dB (W)	η_D (%)
2000	10.2	14.9	48.7	18.8	52.8

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Designed for broadband operation
- Excellent ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{(BR)DSS}$	+40	Vdc
Gate--Source Voltage	V_{GS}	-0.5 to +10	Vdc
Drain Current	I_D	7	A
Power Dissipation(@ T_C = 70 °C)	P_{DISS}	78	W
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+165	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction-Case Thermal Resistance	R_{thJC}	1.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics

Characteristic and Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Voltage V_{GS}=0, I_{DS}=10mA	$V_{(BR)DSS}$		40		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 25V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate-Source Leakage Current (V_{GS} =5 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Quiescent Voltage (V_{DS} = 10V, I_D = 350 mA)	$V_{GS(Q)}$		4.2		V
Drain-Source Voltage (On state) (V_{GS} = 10V, I_D = 1 A)	$V_{DS(ON)}$			0.32	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =12.5 V, f = 1 MHz)	C_{ISS}		57		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =12.5 V, f = 1 MHz)	C_{OSS}		41		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =12.5 V, f = 1 MHz)	C_{RSS}		1.6		pF

Functional Tests (In Innogration Test Fixture, 50 ohm system): V_{DD} = 12 Vdc, I_{DQ} = 350 mA, f =2000 MHz, CW

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain@ P_{OUT}=15W	Gp	8	10		dB
Drain Efficiency@P_3dB	η_D	43	50		%
3dB Compression Point	P_3dB		18		dBm
Load Mismatch, P_{OUT}=15W, All Phase angles	Load Mismatch	20：1			VSWR

TYPICAL CHARACTERISTICS

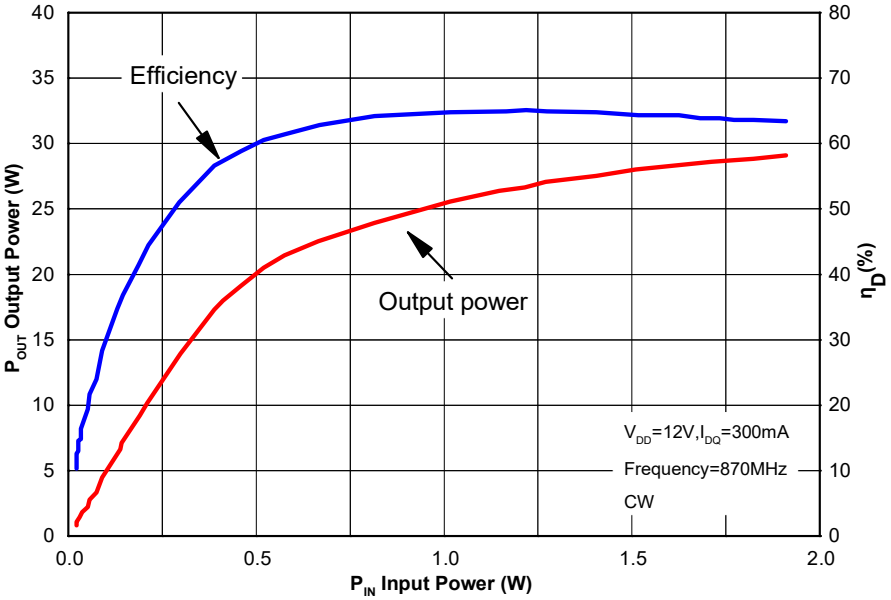


Figure 2. Output power and drain efficiency as function of input power（870MHz）

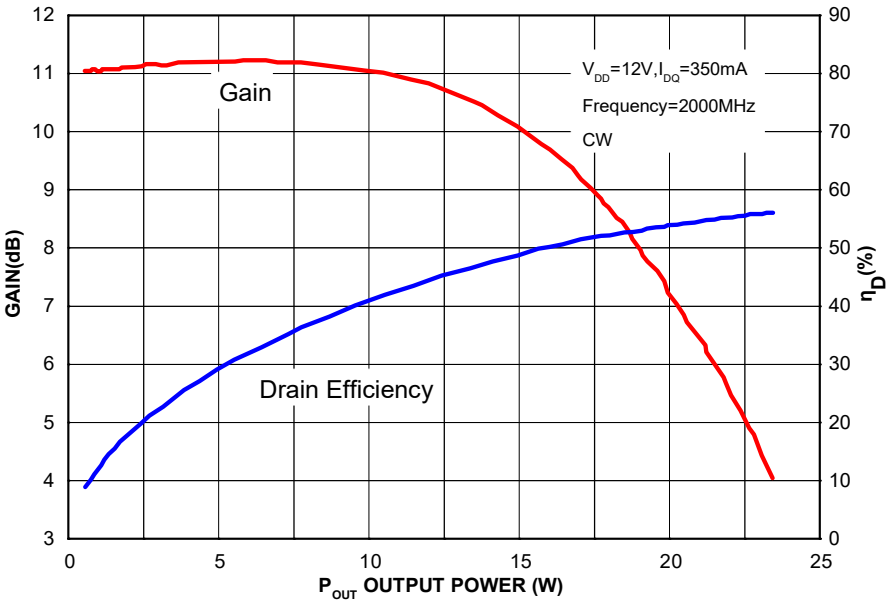
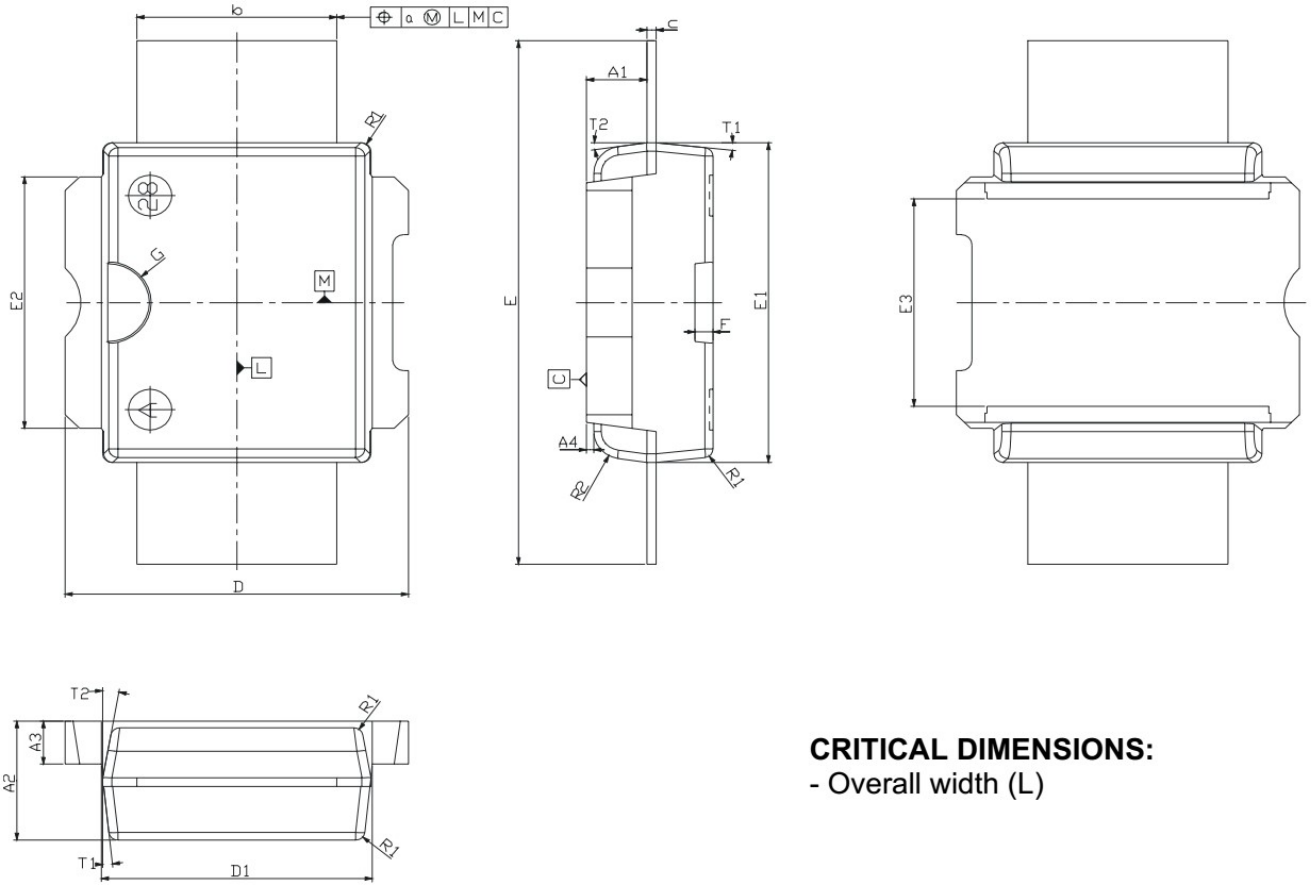


Figure 3. Power gain and drain efficiency as function of output power（2000MHz）

Package Outline

Straight lead package dimensions



CRITICAL DIMENSIONS:
- Overall width (L)

UNIT	A1	A2	A3	A4	a	b	c	D	D1	E	E1	E2	E3	F	G
mm	1.72 1.62	3.6 3.4	1.4 1.2	0.25 0.15	0.2	5.65 5.4	0.32 0.23	9.6 9.4	7.6 7.4	15.65 15.15	9.5 9.3	7.5 7.3	6.3 5.9	0.5	1.2
inches	0.068 0.064	0.142 0.134	0.054 0.046	0.009 0.005	0.007	0.221 0.212	0.012 0.008	0.377 0.370	0.298 0.290	0.615 0.595	0.375 0.365	0.294 0.286	0.247 0.231	0.019	0.047

UNIT	R1	R2	T1	T2
mm	0.25	0.8	6deg	10deg
inches	0.01	0.031	6deg	10deg

Note: Resin protrusions not included (Max. value: 0.15 mm per side)

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-P2-B						23/01/2017

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/01/23	Rev 1.0	Preliminary Datasheet
2017/02/27	Rev 2.0	Product Datasheet

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